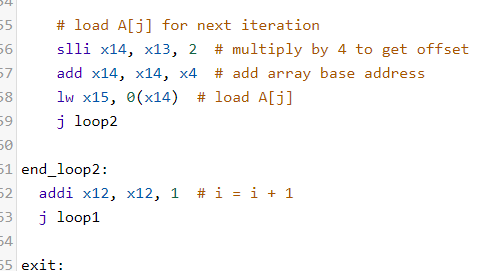
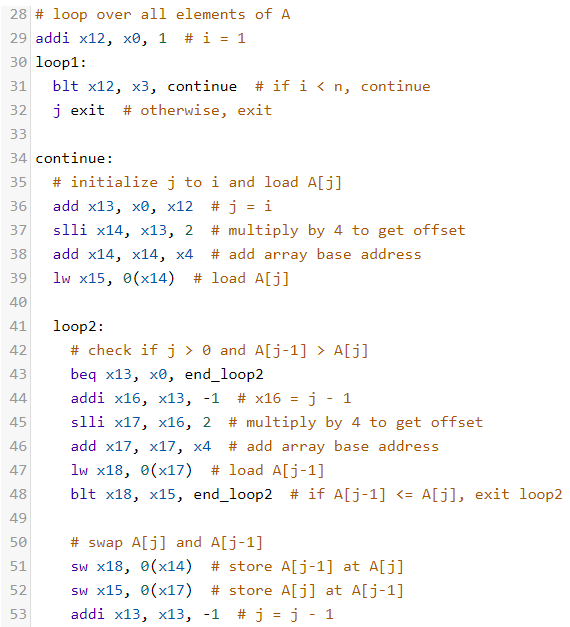
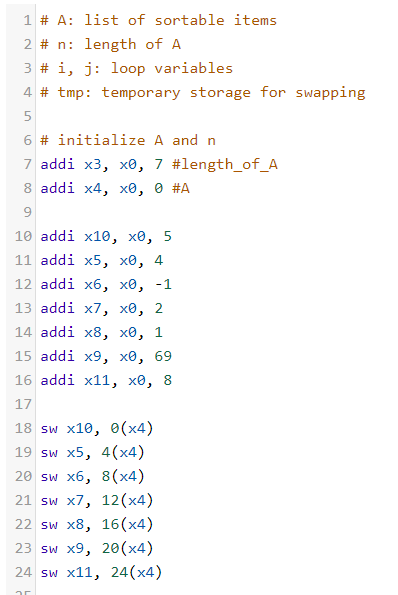
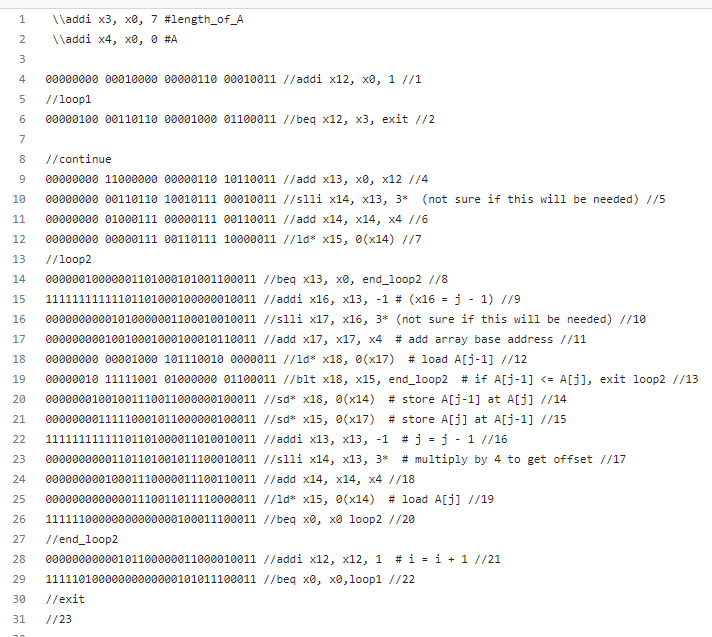
**Insertion Sort (RISC V Assembly)**

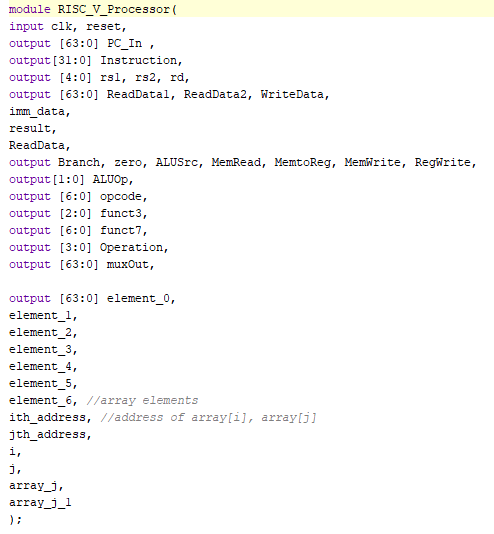
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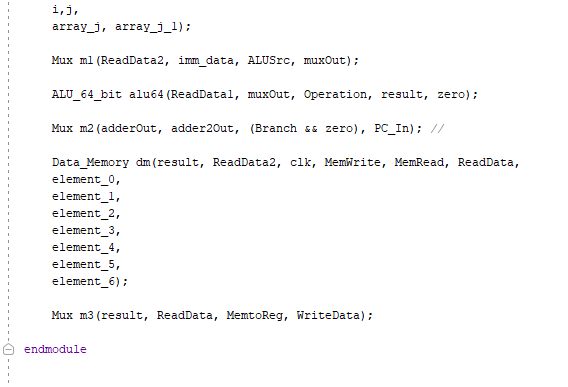
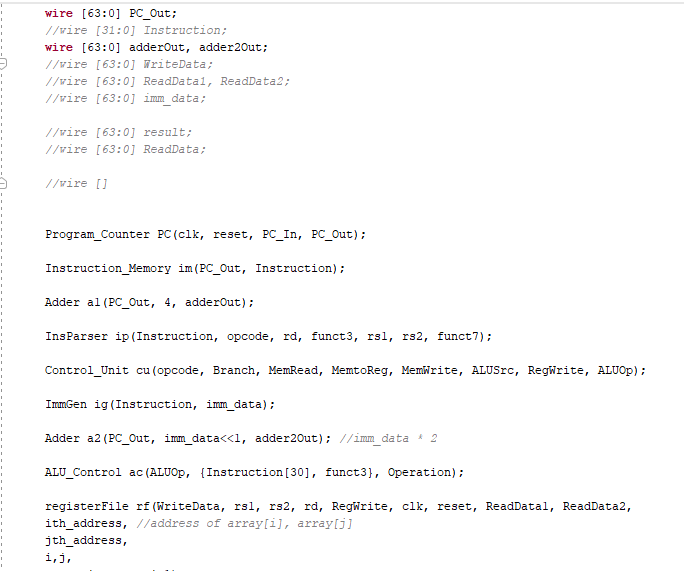
**Decoded Instruction Sort Code into Machine Code**

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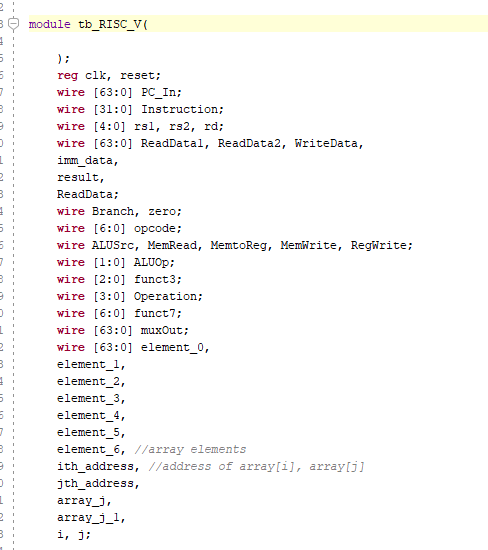
**Single Cycle Processor**

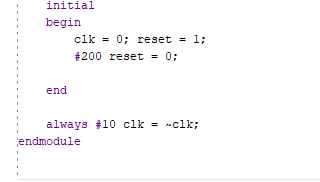
**Top Module**





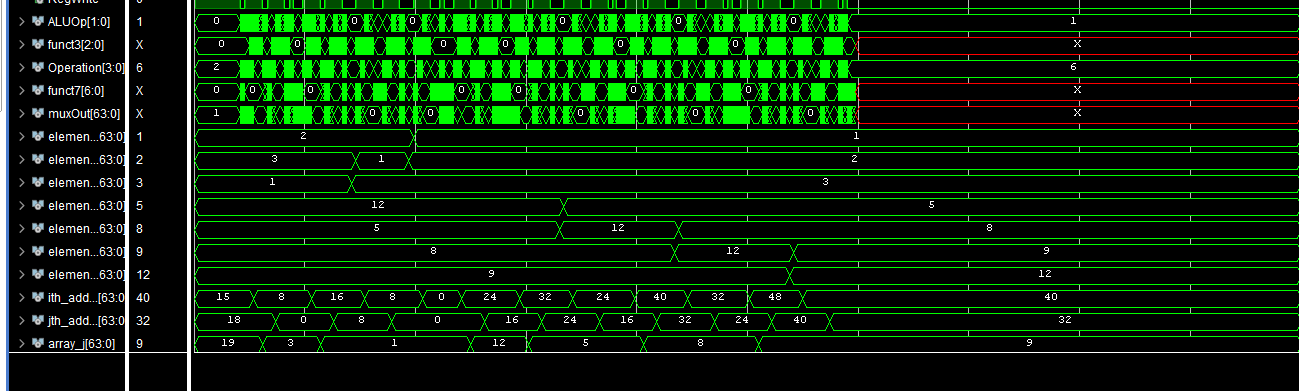
**Test Bench**

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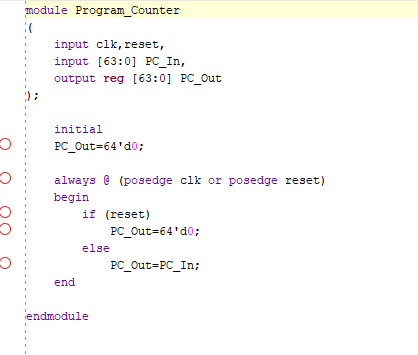
**Wave**

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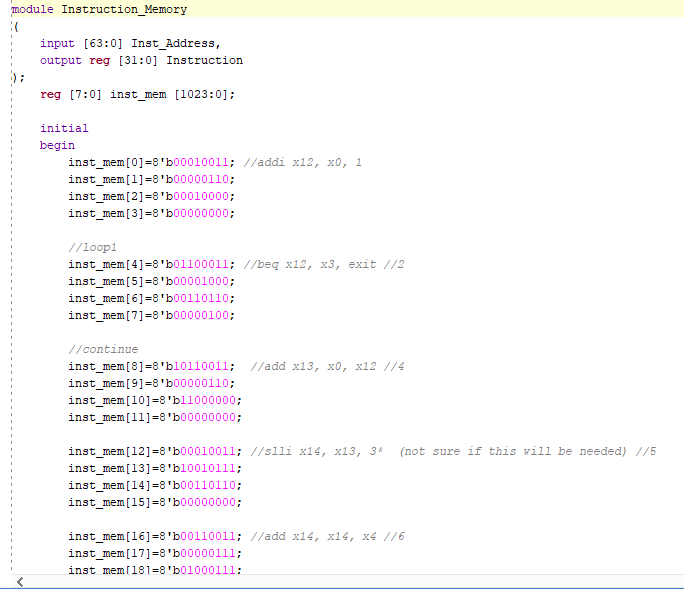
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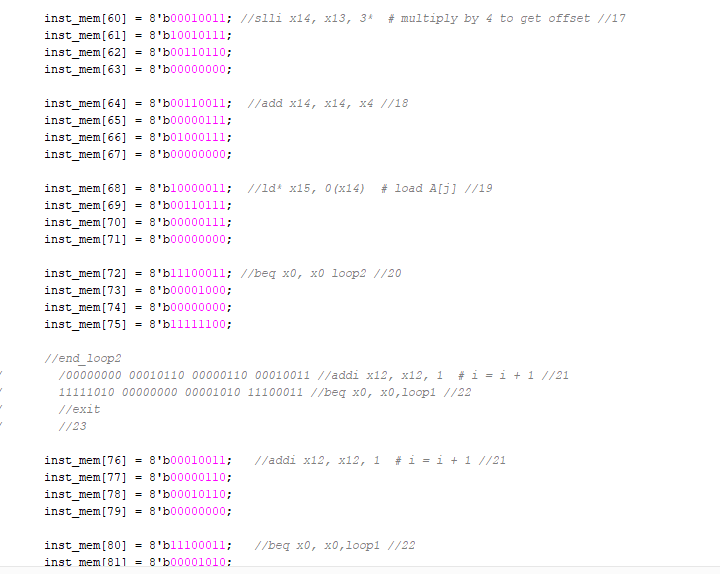
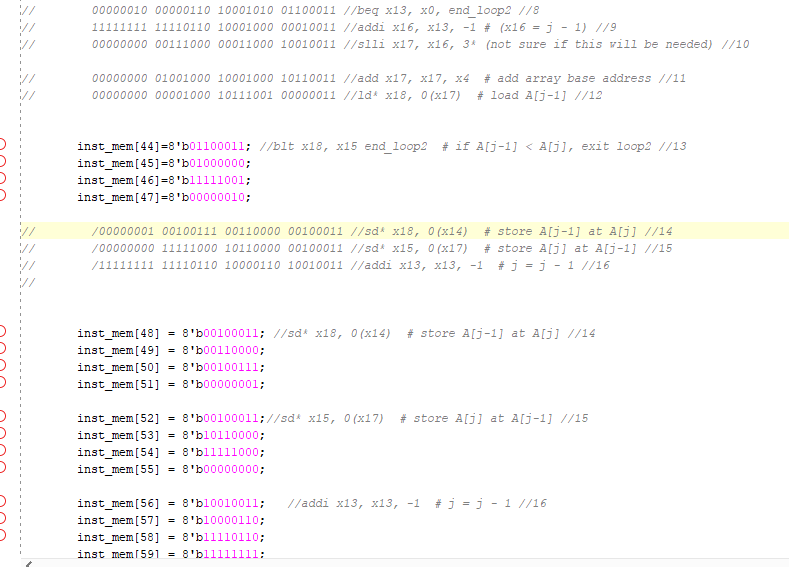
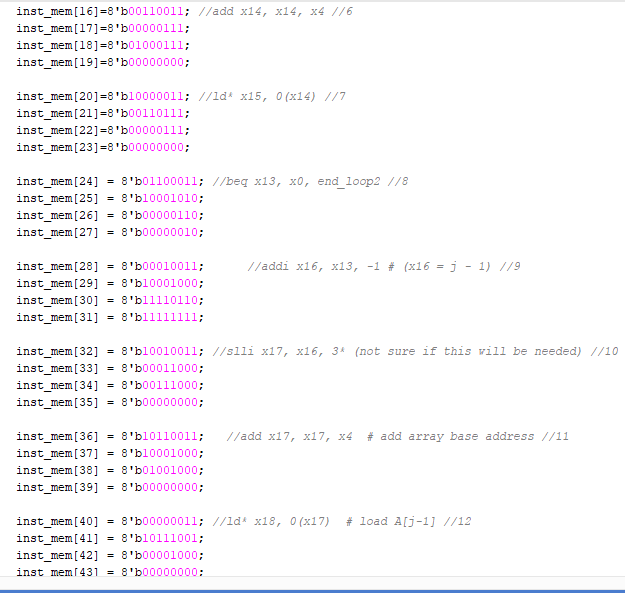
**Intermediate Modules**

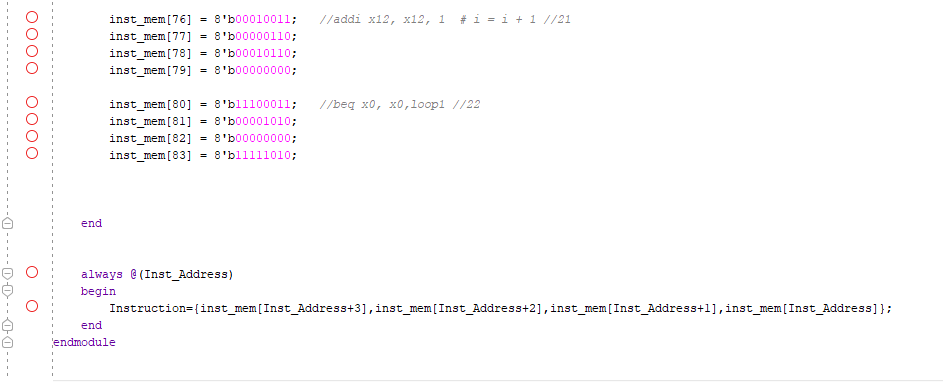
**Program Counter**

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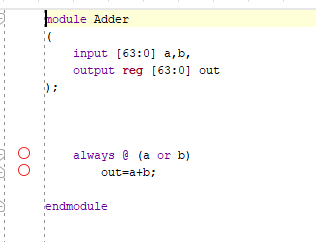
**Instruction Memory**

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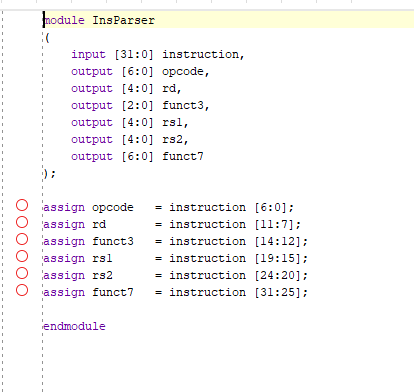
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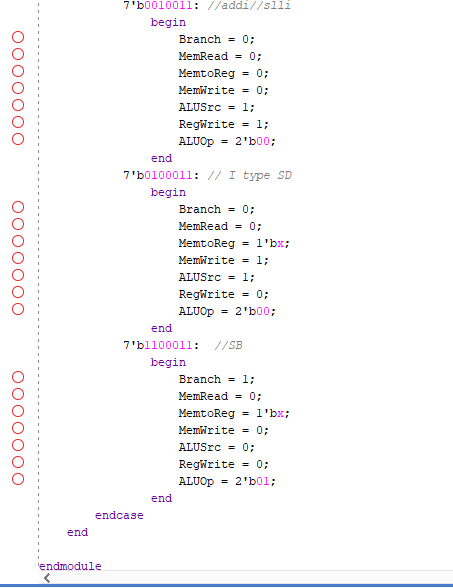
**Adder**

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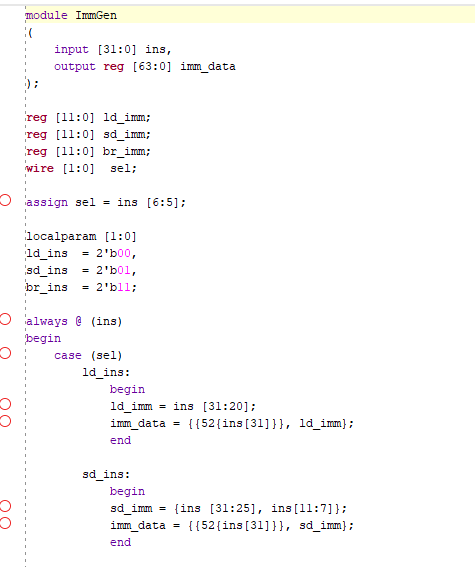
**Instruction Parser**

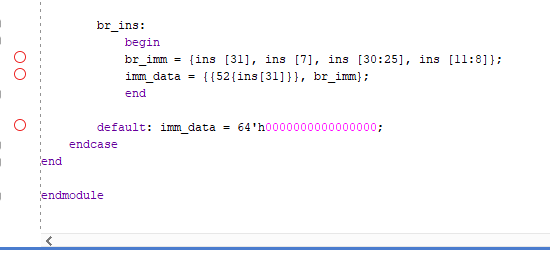
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**Control Unit**

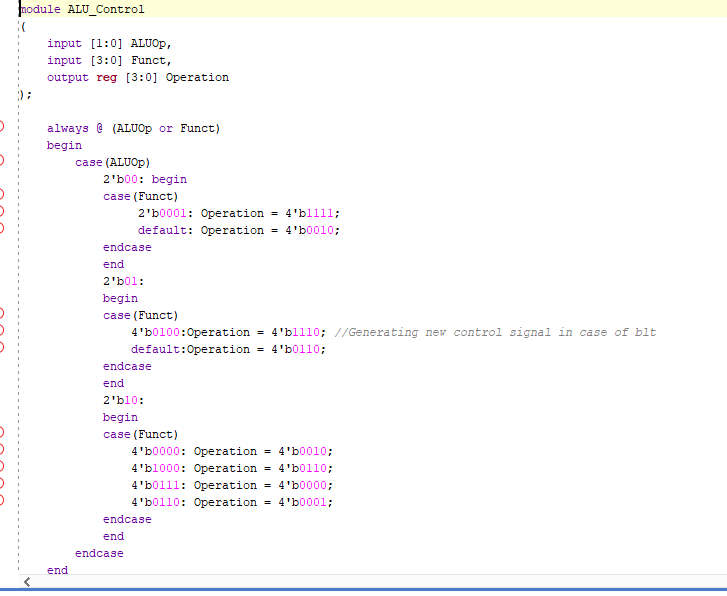
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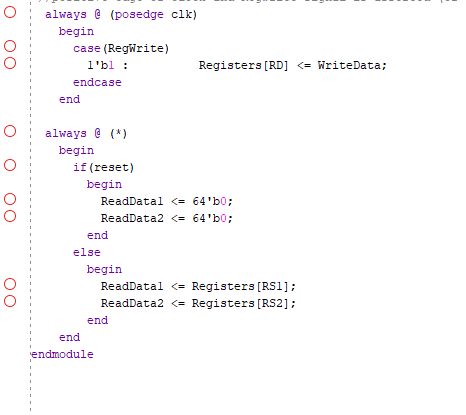
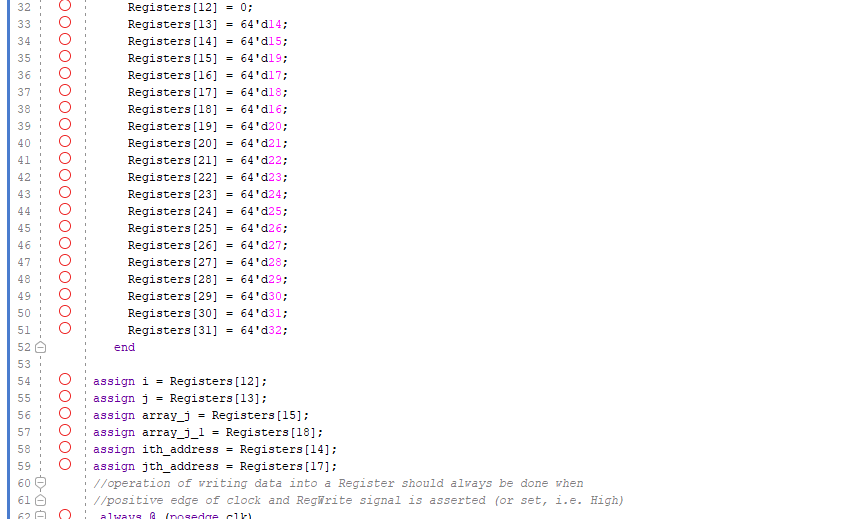
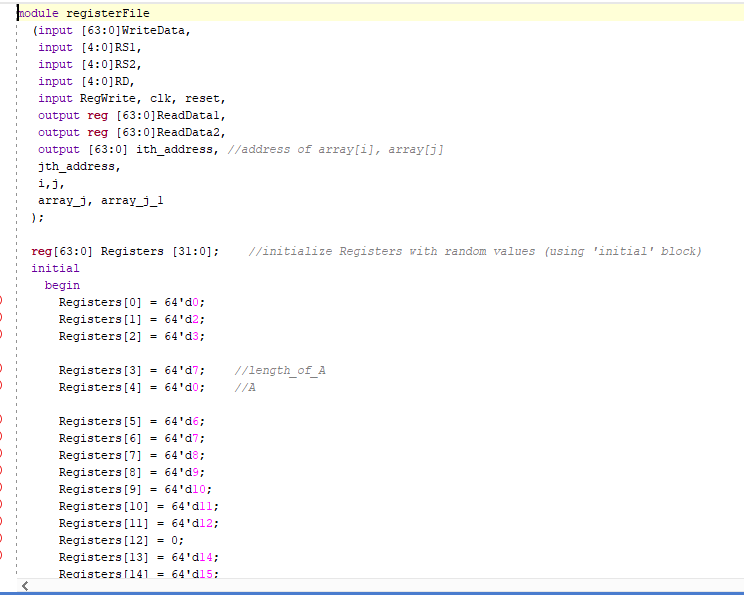
**Immediate Generator**

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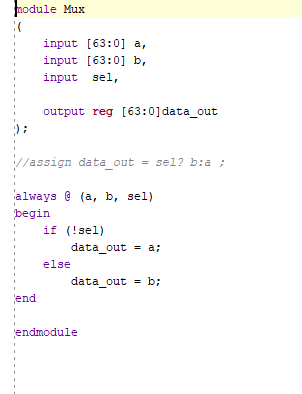
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**ALU Control**

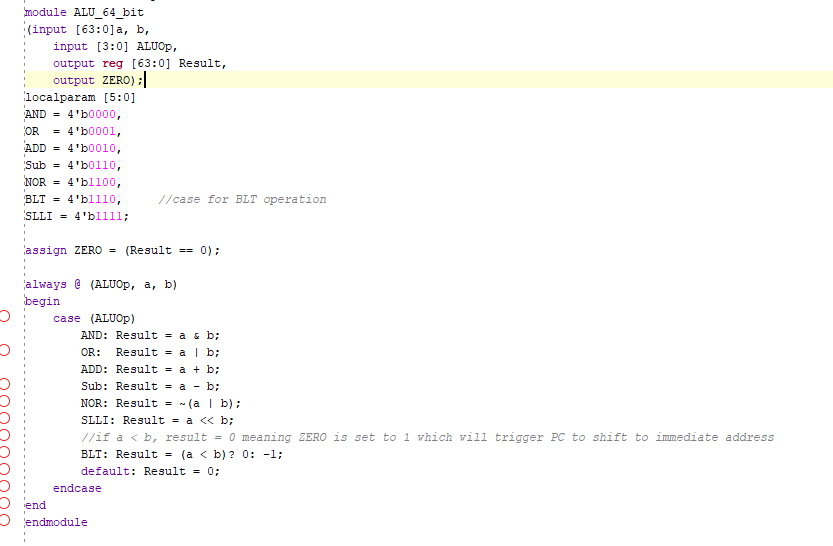
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**Register File**

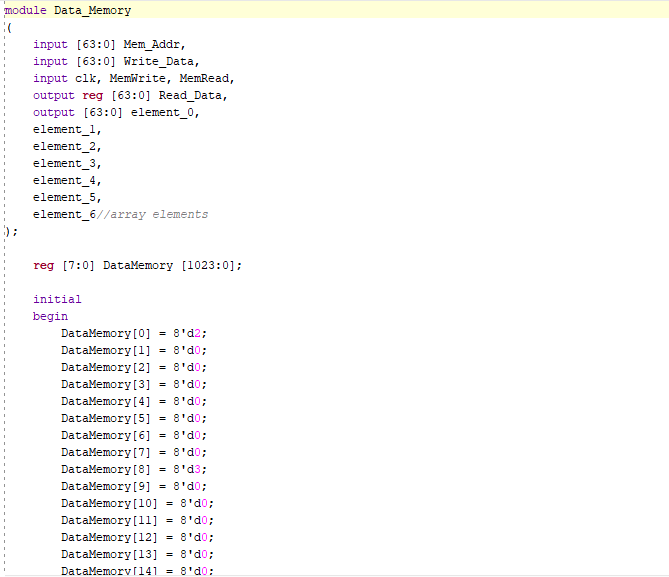
**Mux**

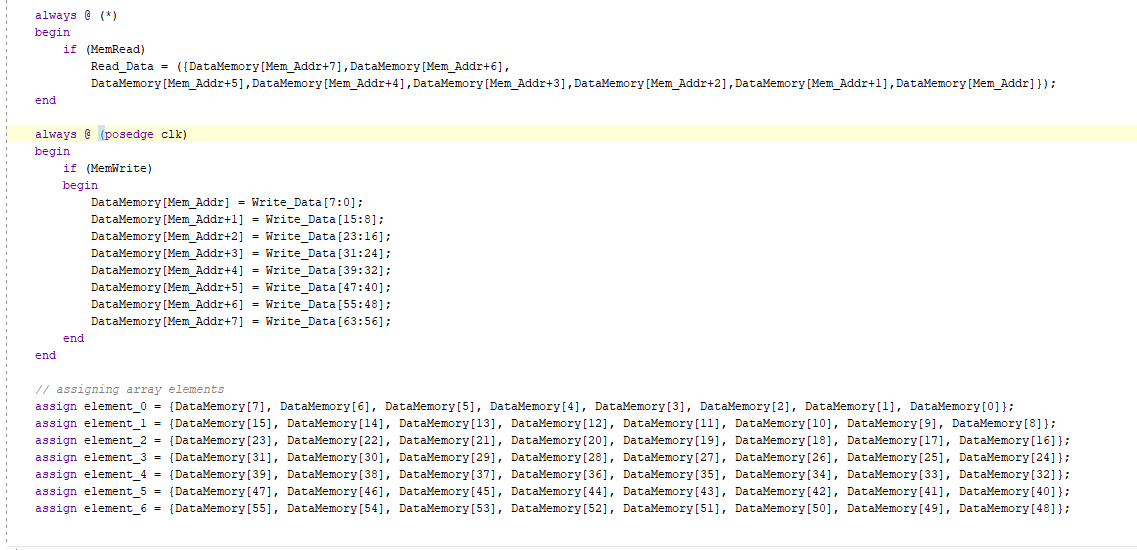
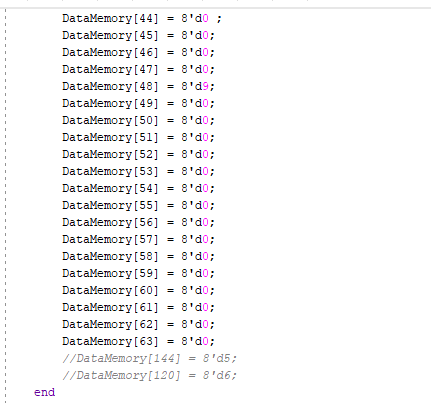
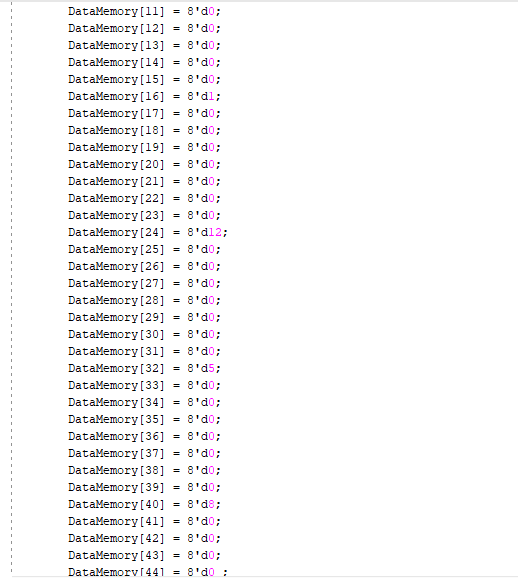
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**ALU 64 bit**

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**Data Memory**

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